REMARKS

No new claims have been added and no claims have been cancelled. No claims have been amended. Claims 1-4 are pending.

Claim Rejections - 35 USC § 103

The Examiner rejects claims 1-4 under 35 USC § 103 as obvious in view of the combination of Bass et al. (USP 6,557,053) and Runaldue (USP 6,067,408). This rejection is respectfully traversed.

A. Introduction

According to MPEP § 2142, to establish a *prima facie* case of obviousness, three criteria must be met: (1) there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; (2) there must be a reasonable expectation of success; (3) the prior art references when combined must teach or suggest all the claim limitations. Importantly, the teaching or suggestion to make the claimed combination must be found in the prior art and not be based on applicant's disclosure. See *In re Vaeck*, 947 F.2d 488 (Fed. Cir. 1991).

Claims 1-4 are not obvious in view of the cited references for multiple reasons.

B. Arguments

First, the cited references may not be properly combined because they are not all in the same field. "In order to rely on a reference as a basis for rejection of an applicant's invention, the reference must either be in the field applicant's endeavor or, if not, then be reasonably pertinent to the particular problem with which the inventor was concerned." MPEP 2141.01(a) quoting *In re*

Oetiker, 977 F.2d 1443, 1446, 24 USPQ2d 1443, 1445 (Fed. Cir. 1992). Pertinent to the pending application is *Wang Laboratories, Inc. v. Toshiba Corp.*, 993 F.2d 858, 26 USPQ2d 1767 (Fed. Cir. 1993) in which the court found that claims directed to single inline memory modules (SIMMs) for installation on a printed circuit motherboard for use in personal computers were not in the same field of endeavor as SIMMs for an industrial controller.

Regarding Bass, the primary reference, and Runaldue, although Bass and Runaldue describe systems that involve data packets, they are nonetheless in different fields. Bass describes a three way memory system having an input and an output FIFO buffer and an external memory. (Bass, 2:13-36) Runaldue describes an interface between two FIFO memories each desiring access to a variable rate storage device. (Runaldue, 6:19-21) Runaldue does not involve a memory system like that described in Bass.

In addition, the patent office has classified Runaldue as pertaining to "bus interface architecture, bus bridge, variable or multiple bus width" in class 710/307 and Bass as pertaining to "peripheral monitoring, status updating" in class 710/19, showing that the patent office considers the teachings of Bass and Runaldue to be in different fields.

For these reasons, Bass and Runaldue are in different fields and may not be properly combined.

Second, because Bass may not be properly combined with Runaldue, Bass alone must be considered. The Office Action admits that various limitations recited in claim 1 are not taught by Bass alone, and, therefore, the Office Action adds Runaldue to the rejection. Therefore, because Runaldue may not be properly combined with Bass as set forth above, and in view of the admissions recited in the Office Action, Bass does not alone teach all of the limitations recited in claim 1. Therefore, claim 1 is not rendered obvious by Bass.

Third, the Final Office Action states that:

> One skilled in the art would have recognized delivering data packets at a relatively slow rate to a plurality of switching elements whereby some latency occurs between said data packets, and would have applied Runaldue et al.'s buffer management system for use in interfacing between asynchronous components, such as local area network and a storage drive with variable latency in Bass et al.'s management of queues of data being received from an outside source and inputted into a device for further processing. (p. 3 of the Final Office Action)

However, the Office Action fails to explain a basis as to why or how one skilled in the art would have made this described recognition. Further explanation is requested.

Fourth, there is no motivation to combine the references expressed in the cited art. "The mere fact that references can be combined or modified does not render the resultant combination obvious unless the prior art also suggests the desirability of the combination." MPEP 2143.01 citing *In re Mills*, 916 F.2d 680 (Fed. Cir. 1990) (emphasis in MPEP). As set forth above, because Bass and Runaldue are not in the same filed, there is likewise no motivation to combine inventions from disparate areas. (Moreover, if the teachings described in Bass and Runaldue were combined, a unique device unlike that recited in claim 1 would result.)

More specifically, the Office Action asserts that Rumaldue provides the motivation to combine Runaldue with Bass because Runaldue states that a more efficient buffer management system is needed. (Runaldue, 2:2:49-54) However, this portion of Runaldue merely provides the motivation for the disclosure made in Runaldue. (Runaldue, 2:2:49-54) Runaldue teaches an interface between two FIFO memories each desiring access to a variable rate storage device (Runaldue, 6:19-21) The motivation in Runaldue is to more efficiently manage competing access to a variable rate devices. However, this motivation is not applicable to Bass. This is because Bass does not involve competing component access to a variable rate device. Rather, Bass involves a

memory system with a manager. As such, the stated motivation for the system in Runaldue does not serve as motivation for the combination of Runaldue and Bass.

Fifth, Bass and Runaldue are not properly combinable as the FIFO buffers in Runaldue and Bass serve different purposes and can not be combined. Runaldue teaches a system with two FIFO buffers: a receive FIFO 52 in which data received from network interface 50 are stored; and a transmit FIFO 54 in which outgoing data are received and stored before being presented to a network interface 50. (Runaldue, 4:18-25) That is, each of the Runaldue FIFO buffers serves a different purpose form the other. In contrast, the FIFO buffers in Bass are used in combination for the sole, uniform purpose of receiving incoming data, even though they are referred to input FIFO buffer 14 and output FIFO buffer 32. (Bass, 2:13-36) As such, the systems described in Bass and Runaldue are different and incapable of combination.

Sixth, if *in arguendo*, Bass were combinable with Runaldue, the switching elements recited in the claim are not taught or suggested by this combination. Because Bass teaches a three way memory system having an input and an output FIFO buffer and an external memory (Bass, 2:13-36) and Runaldue teaches an interface between two FIFO memories each desiring access to a variable rate storage device (Runaldue, 6:19-21), their combination does not yield a device that includes all of the claimed limitations. Neither Bass nor Runaldue include the switching elements recited in claim 1. As such, even if Runaldue were combined with Bass, the resulting creation would be different from and would not teach or suggest the switching elements (and other limitations) recited in claim 1.

Seventh, Runaldue does not teach what the Office Action asserts. The Office Action asserts that Runaldue discloses "delivering data packets at a relatively slow rate to a plurality of switching elements whereby some latency occurs between said data packets." (Final Office Action, p. 3, lines 8-10) However, the cited portions of Runaldue do not teach or suggest "delivering data packets at a

relatively slow rate to a plurality of switching elements whereby some latency occurs between said data packets." The cited portions of Runaldue merely state:

(1) that computers send data at a fixed rate while storage devices operate at a variable rate (Runaldue, 1:59-65);

(2) that a system bus interconnects an interface adapter, a storage device, a CPU, and other peripheral devices; and

(3) that there is a need for efficient buffer memory management for a device that interfaces both to a LAN and a storage device. (2:50-53)

Therefore, the cited portions of Runaldue and the entire reference fail to teach or suggest "switching elements" and "a head FIFO memory for sequentially delivering data packets at a relatively slow rate to a plurality of switching elements whereby some latency occurs between said data packets" as recited in claim 1.

The Examiner admits that Bass fails to disclose "delivering data packets at a relatively slow rate to a plurality of switching elements whereby some latency occurs between said data packets." (Final Office Action, p. 3, lines 6-8) Runaldue fails to cure this deficiency. As such, the combination of Runaldue and Bass fails to teach the limitations recited in claim 1. The Office Action fails to present a *prima facie* case of obviousness.

For all of the reasons set forth above, claim 1 is not rendered obvious by the cited prior art patents. By virtue of their dependency on claim 1, claims 2, 3 and 4 are likewise patentable over the cited prior art patents.

Conclusion

In view of all of the above, it is respectfully submitted that the application is in condition for allowance. Reconsideration and reexamination are respectfully requested and allowance at an early date is solicited. The Examiner is invited to call the undersigned attorney to with any questions or to discuss any steps necessary for placing the application in condition for allowance.

Respectfully submitted,

Date: July 20, 2005

Mark A. Goldstein, Reg. No. 50,759

SoCal IP Law Group
310 N. Westlake Blvd., Suite 120
Westlake Village, CA 91362
Telephone: 805/230-1350
Facsimile: 805/230-1355
email: mgoldstein@socalip.com